JOURNAL OF MODERN SCIENCE
SPECIAL ISSUE
3/57/2024
www.jomswsge.com

DOI: doi.org/10.13166/jms/191420

IWONA SZUSTER
WSEI University in Lublin, Poland
ORCID iD: orcid.org/0009-0001-0444-2397

MARIUSZ MAZUREK
Institute of Philosophy and Sociology of the Polish Academy of Sciences, Poland
ORCID iD: orcid.org/0000-0002-9646-6897

DARIA STEFAŃCZAK
WSEI University in Lublin, Poland
ORCID iD: orcid.org/0009-0003-6297-3473

KONRAD GAUDA
WSEI University in Lublin, Poland
ORCID iD: orcid.org/0000-0002-7300-6978

OPTIMIZATION OF ALGORITHMS FOR EFFECTIVE MANAGEMENT OF THE MEASUREMENT PROCESS IN ELECTRICAL IMPEDANCE TOMOGRAPHY AND ULTRASONIC TOMOGRAPHY

OPTYMALIZACJA ALGORYTMÓW DLA EFEKTYWNEGO ZARZĄDZANIA PROCESEM POMIARU W ELEKTRYCZNEJ TOMOGRAFII IMPEDANCYJNEJ I TOMOGRAFII ULTRADŹWIĘKOWEJ

Abstract

The article discusses the design of advanced embedded algorithms that aim to manage and control the measurement process using the Electrical Impedance Tomography and Ultrasonic Tomography methods. The project aims to develop solutions that optimize the performance of embedded devices that must operate on limited resources such as memory, computing power, or bandwidth. Minimizing energy consumption is an important aspect, especially for battery-powered devices. Algorithms must also be adapted to specific hardware constraints, such as low RAM or CPU limitations, which require complex engineering and optimization. Additionally, the project assumes the implementation of algorithms that consider security aspects, which is crucial in protecting data processed and transmitted by the device. It also requires the development of effective communication methods between the embedded device and other systems, including appropriate communication protocols.

Streszczenie

Artykuł omawia projektowanie zaawansowanych algorytmów wbudowanych, które mają na celu zarządzanie i kontrolę procesu pomiaru metodą Elektrycznej Impedancji Tomografii (EIT) oraz Tomografią Ultradźwiękową (UST). Celem projektu jest opracowanie rozwiązań optymalizujących wydajność urządzeń wbudowanych, które muszą działać na ograniczonych zasobach takich jak pamięć, moc obliczeniowa czy przepustowość. Ważnym aspektem jest minimalizacja zużycia energii, co jest szczególnie istotne w przypadku urządzeń zasilanych bateryjnie. Algorytmy muszą być także dostosowane do specyficznych ograniczeń sprzętowych, takich jak mała ilość pamięci RAM czy ograniczenia procesora, co wymaga skomplikowanej inżynierii i optymalizacji. Dodatkowo, projekt zakłada implementację algorytmów z uwzględnieniem aspektów zabezpieczeń, co jest kluczowe w kontekście ochrony danych przetwarzanych i przesyłanych przez urządzenie. Wymaga to również opracowania skutecznych metod komunikacji między urządzeniem wbudowanym a innymi systemami, co obejmuje stosowanie odpowiednich protokołów komunikacyjnych.

Keywords: *ultrasonic imaging, sensors, measurements*

Słowa kluczowe: *obrazowanie ultradźwiękowe, sensory, pomiary*

Implementation of algorithms and methods

The main goal of the work was to develop solutions that optimize the performance of embedded devices. The solution was based on Electrical Impedance Tomography (EIT) and Ultrasonic Tomography (UST). The project involves the implementation of algorithms and the development of effective methods of communication between the built-in device (Nowakowski et al., 2017; Romanowski et al., 2019; Soleimani et al., 2009).

Measurement and data processing occur in parallel when some of the functional blocks perform tasks involving the acquisition of measurement data. At the same time, data obtained during the previous sequence is processed. Using such a solution allows for optimization of the solution's performance, which contributes to increasing the developed solution's efficiency and speed of operation (Rymarczyk et al., 2019; Rymarczyk et al., 2018).

Processing the measurement signal in the described system is a step-by-step process that starts immediately after triggering the measurement signal (ADC_CNV_START). The first step is to capture signal samples, the amount of which is determined by the duration of the synchronization signal (SYNC). This time corresponds to a multiple of the duration of the excitation signal period. The collected samples are then saved in the device's cache.

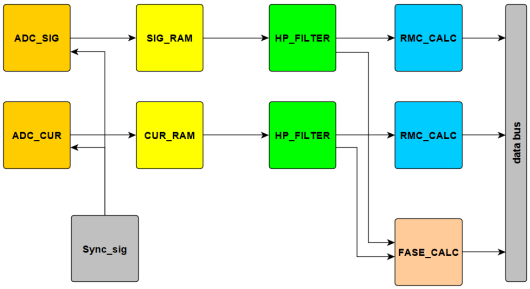
In the second stage of the process, the signal is filtered to eliminate the DC component. To do this, the signal passes through a digital high-pass filter, which helps remove unwanted frequencies.

Then, the pre-processed signal is directed to two parallel processing blocks. The first is the RMS (Root Mean Square) value calculation block, which determines the practical signal value. The second block calculates the phase shift value, which is crucial for further analysis of the signal characteristics.

At the end of the process, the measured and processed data are presented as values corresponding to the obtained parameters. This data is displayed on the system bus, and the entire process ends with generating a measurement readiness signal (ADC_CNV_CPL), signaling the end of the measurement cycle.

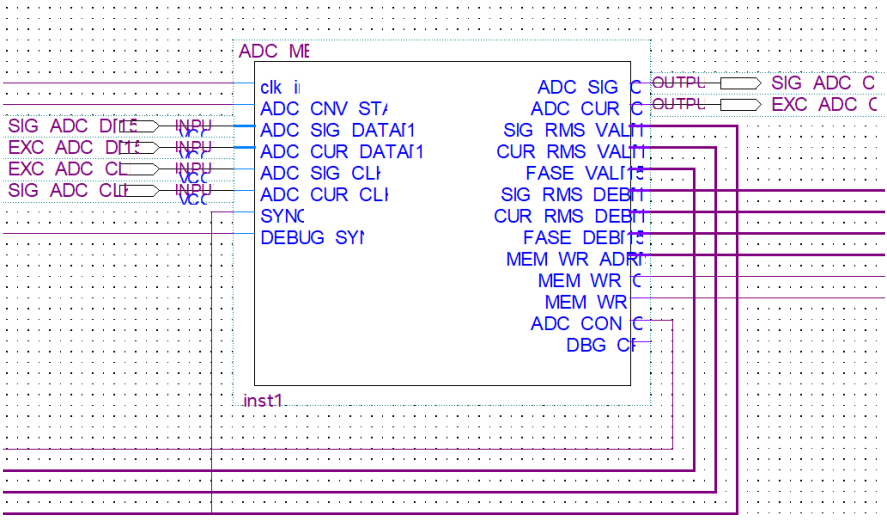
The interactions between the system's functional blocks are detailed in Figure 1, allowing for a better understanding of signal flow and processing throughout the system.

Figure 1. *ADC_SIG block diagram*



One element that plays a vital role in the measurement process is the ADC_CTR block. This block deals not only with acquiring and sampling measurement data but also with processing and filtering the acquired data until measurement results (RMS signal value, RMS current value, phase shift value) are obtained. The communication method of the measuring block is shown in Figure 2.

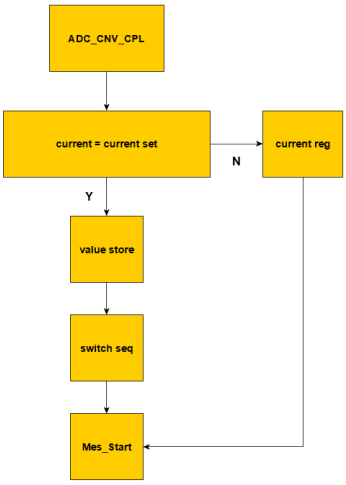
Figure 2. *Connection graph of the measuring block*



The MES_PRC_CTR block in the measurement system plays a vital role as a controller of the measurement process. Its primary function is to manage and coordinate the operation of individual functional blocks, determine the required parameters, and synchronize the entire measurement process. The control process starts by starting the measurement by issuing the Mes_Start signal. After completing the measurement stage and receiving the ADC_CNV_CPL readiness signal, the system analyzes the collected data. If the measured excitation current values are within the permissible error limits, the data is written to the external RAM. The system then moves the measurement sequence to the next defined position, and the process starts again.

If the measured current value does not meet the established acceptance criteria, the system initiates a digital adjustment process, which results in repeated measurement. Figure 3 illustrates the entire control process and its stages. It shows a block diagram of the operation of the measurement control system. This diagram visualizes the signal flow and the control hierarchy within the system, which is essential to understanding the functioning and interactions between components.

Figure 3. *Block diagram of the measurement process control mechanism*



Carrying out tests of the developed algorithms

The process of testing algorithms and embedded software, crucial to ensuring the effective operation of FPGA-based systems, begins with a series of test stages necessary to verify and optimize every aspect of the device's operation.

The first step in this process is simulations. Before implementing an actual FPGA, the software is thoroughly tested using HDL simulation tools such as VHDL or Verilog. This phase allows you to precisely check the correctness of the project's logic and functionality, eliminating initial errors before loading the software onto the device.

Then, unit tests are performed, which focus on analyzing individual project components or modules. These tests allow for the early identification and correction of errors, which is necessary to ensure the stability of basic system functions.

After completing unit tests, the system goes through the integration testing stage. In this phase, it is checked whether all modules work together correctly, which is critical for the entire system's functionality. Then, functional tests confirm that the FPGA system meets all the requirements, especially under various operating conditions.

Performance testing is also crucial, especially if the system has specific speed, throughput, and latency requirements. Additionally, load tests are performed to examine how the FPGA system copes under maximum load conditions. These tests are important for assessing the system's stability, resistance to high temperatures, and potential power supply problems.

The final stage is testing and debugging on real hardware. Loading the software onto an actual FPGA device and testing it in real-world conditions allows for final verification of system performance, confirming that the implementation on real hardware is working as expected.

Such a detailed and multi-stage testing process ensures that the FPGA system is thoroughly tested and ready to operate effectively in practical applications, fully considering all key functionalities.

Tests of the mechanisms of the measurement and data processing block

Several tests and simulation analyses were performed as part of the tests to check the correctness of the obtained data and the integrity of the time compatibility of individual signals. The work began with a simulation using synthetic data generated by a specially created function block simulating the operation of an analog-to-digital converter, based on which the correctness of the obtained results was analyzed.

The second testing stage focused on testing the finished solution using the target hardware layer and specially adapted embedded software containing functions and procedures necessary for debugging. To test the correctness of the operation, it is essential to create mechanisms enabling the transfer of selected, measured signal waveforms to an external environment. For this purpose, the measurement function block was expanded with a debugging side, allowing for recording the envelope of the measured signal, expanded with a set of 3 two-port RAMs. The next step to check the correctness of the obtained results was to compare the solution with a standard signal generator and use laboratory measuring instruments. The obtained envelope results and calculated RMS values were compared with the values obtained using measuring instruments. As part of the solution tests, test procedures were created to check the correctness of written and read data and data segregation in virtual non-volatile memories. For this purpose, a function block was designed to simulate the operation of the ADC_MES block, replacing accurate data with synthetic data. Then, the obtained data were analyzed to ensure its correctness.

Tests of data storage and segregation mechanisms and forcing signal generation/current regulation system

As part of the solution tests, test procedures were created to check the correctness of written and read data and data segregation in virtual non-volatile memories. For this purpose, a function block was designed to simulate the operation of the ADC_MES block, replacing accurate data with synthetic data. Then, the obtained data were analyzed to ensure its correctness. The set

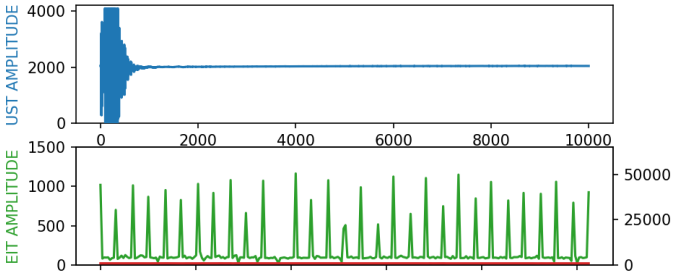
of excitation signal-generating blocks was analyzed in the stage of analyzing the correct operation of the excitation signal-generating blocks, and individual function blocks were simulated and tested for the correctness of the generated waveforms. Then, the correct operation of the entire excitation generation and control unit was analyzed. In the first phase of the tests, the proper operation of the signal generation system was checked. For this purpose, various frequencies of the excitation signal were synthetically set, and the correctness of the obtained frequencies was checked using measuring instruments. The level of signal mapping with expected values was also analyzed. In the next phase, the correct operation of the signal amplitude control block was checked by setting successive values of the forcing amplitude and then analyzing the results using reference devices. The last functional testing phase was to check the correct operation of the entire function block.

Measurement system

The lower urinary tract tomograph has been tested for system stability (Fig. 4). For this purpose, test software was prepared and launched to force the measurement of UST and EIT as often as possible. The test was intended to test the device in extreme conditions that the end user could not enforce during everyday use. The test software was parameterized to perform 10,240 measurements. All measurements were performed correctly (Fig. 5).

Figure 4. *A tomograph for examining the lower urinary tract while assessing the stability of the system*

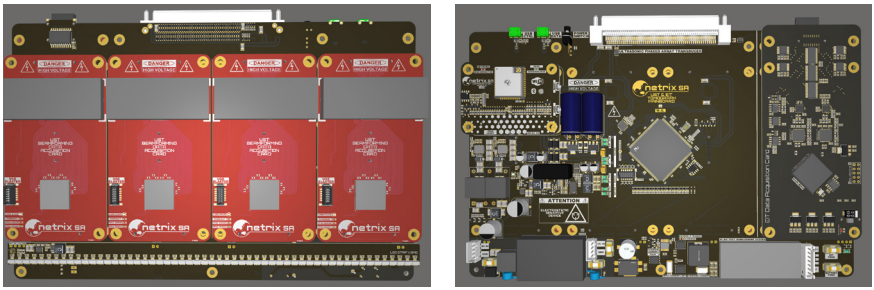
Figure 5 *Test measurement of UST (top) and EIT (bottom)*



The device has undergone several design changes, the main one being a complete change in its form and method of use. The new design assumes the construction of a device as a portable backpack connected to textile underwear equipped with a miniaturized ultrasonic head and electrical impedance measuring electrodes. The new type of construction compromises mobility, comfort of use, and the quality of diagnostics. The electrical design of the device has been optimized in terms of energy consumption. The power supply section has been rebuilt, including it is equipped with a separating converter that isolates the patient from the power grid when it is charged from a charger, new high-voltage converters with better efficiency for generating the forcing signal of ultrasonic transducers in SEPIC technology, and the possibility of installing a galvanically isolated converter. The method of powering measurement cards has also been changed. The new design allows you to disconnect the power supply when inactive, translating into longer battery life. In addition, a Li-Ion battery charger with a BMS system is integrated into the device's motherboard, described in detail in the next section of this report. Below is the new electrical design of the device's main board for dual diagnostics of the lower urinary tract, along with partial assembly work (Fig. 6).

The new design has also been adapted to wireless communication. Using the ESP32 system, a communication module was designed and manufactured, with the possibility of communication via the USB port. Below is the electrical design of the WiFi module, along with 3D models of the boards and a photo of the assembly.

Figure 6. *Design of the tomograph motherboard – bottom view – with UST measurement cards and LED strip installed (a) and design of a tomograph plate – top view – with a WiFi card and an EIT measurement card installed (b)*



(a) (b)

The casing design of the mobile urinary tract diagnostic device was designed in the form of a backpack. This solution ensures patient comfort and ease of wearing without limiting the device's functionality. Sketches of a pattern were made for sewing the textile rear element of the *backpack* along with shoulder straps that will hold the device stably. A ventilation system (using foam and spacer mesh) and an adjustment system (buckles and clamp adjusters) were designed. Textile materials have been carefully selected to ensure both durability and comfort (ventilation, no body contact with the housing body). A vital aspect considered at the conceptual stage was the possibility of cleaning and disinfecting all elements.

Several actions were taken to optimize the comfort of use and functionality in designing a new casing for the device, which will be adapted for children. The case size has been reduced as much as possible to accommodate the smaller dimensions of the electronics while maintaining a flat surface against the back. This solution was used because the anatomical structure of a two-year-old's back is significantly different from that of an eighteen-year-old, which makes it impossible to adapt to their curvature. To increase wearing comfort, foam, and spacer mesh are used on the back of the casing and shoulder straps, which improves air circulation and reduces pressure on the child's back.

Another important element is the battery, the cells of which are arranged so that the device's weight is evenly distributed. Additionally, the battery module

has been designed so that it can be easily unscrewed and the cells removed, allowing them to be replaced.

The housing also has specially designed harness holders, which ensure stable device attachment. The design also includes holes for connectors such as EIT, UST, power, or USB, as well as buttons and mounting holes, which facilitate the installation of additional elements and ensure easy maintenance.

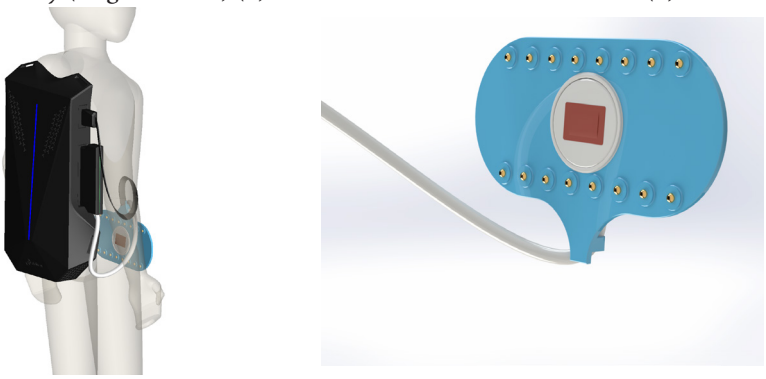
Additionally, ventilation holes have been designed in the housing to optimize the device's operation and prevent it from overheating. These holes ensure adequate air circulation, which is crucial for maintaining the device's proper operating temperature and avoiding overheating electronic components.

The housing also includes a place for an LED strip, which has been integrated to complement the geometry of the new housing, adding an aesthetic and functional visual element.

The entire project focuses on ensuring comfort, safety, and efficiency of use, which is crucial for devices intended for younger users.

To illustrate the device's size on the patient, a visualization was created that shows the body model of a child aged 3-4, 100 cm tall. This visualization helps understand the proportions of the device to the structure of the target patient example. Every effort has been made to provide an ergonomic shape that will fit the contours of the child's body to ensure maximum comfort and freedom of movement. Harnesses with buckles allow for precise adjustment of the device to the patient. The design of the electrode insert, which is an integral part of the measurement system, has been improved. The insert has an electrode system whose arrangement is optimized for EIT and UST measurements. The electrode insert allows easy and safe connection to the measurement system (Fig. 7).

Figure 7. *Visualization of the device housing, connectors, cables, and electrode insert on a human body (height 100 cm) (a) and insert with detached UST head (b)*



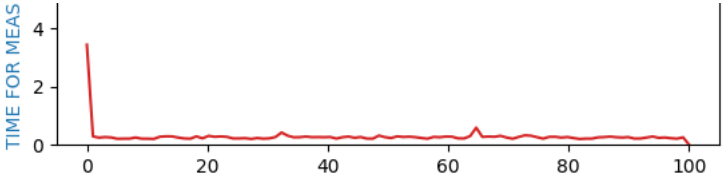
(a) (b)

Assessment of prototype functionality

The aim was to perform a performance test of the device. This test was performed using test software that forces the tomograph to achieve maximum performance using a Wi-Fi wireless network.

One hundred measurements were made, and the execution time was 31 seconds, which means that the average measurement duration is 0.31 seconds, i.e., an average of 3 measurements per second (Fig. 8).

Figure 8 *Series of 100 measurements – duration of a single measurement [s]*



Then, the entire system was validated with the introduced modifications. Before final certification, the tomograph for examining the lower urinary tract was tested as part of the design tests. Four tests were carried out on (1) conducted emissivity, (2) electromagnetic compatibility, (3) immunity to electromagnetic interference, and (4) resistance to ESD discharges.

Conducted emission tests did not reveal any interference exceeding the permissible standards from the device charger to the network. Electromagnetic compatibility tests were carried out in the 30MHz-1GHz band; the tests allowed to locate sources of electromagnetic field exceeding the permissible standards. The problems were mainly due to insufficient filtering of signals entering the device through the cabling. During the tests, the problems found were successively eliminated, and the measurements were repeated until the emission sources that exceeded the standards were removed entirely. The test was completed with a correct result, and the modifications introduced in the device's structure were included in the electrical design. During the electromagnetic interference resistance tests, the tomograph was disturbed by a field with an intensity of 10V/m at a frequency of 80MHz-6GHz in two antenna polarizations. This test was aimed at checking whether the electromagnetic field could disrupt or interrupt the operation of the device. The examination revealed that with one of the antenna polarizations, there are problems with the proper operation of the tomograph. The cause of these problems was the LED strip on the front of the device, which induced noise and passed it on to the motherboard microcontroller. This problem was also solved on-site by installing a ferrite bead on the cable connecting the LED strip and the motherboard. The test was ultimately carried out with a positive result. The last test performed on the CT scanner was resistance to ESD discharges. The device was repeatedly tested at voltages of 8kV and 15kV from every possible side. The discharges were also directed toward the EIT electrodes and the UST head. The device without USB service cables connected worked continuously during these tests. In the case of connected USB service cables, problems with wired communication occurred already at an 8kV surge. In the case of these tests, this is an acceptable situation. The device may have trouble communicating with the external system but should be ready to resume transmission without a power reset. These problems could not be repeated during the final certification tests because all communication is carried out only via Wi-Fi, and the end user needs access to the service USB ports.

After the design tests, several modifications were made to the device's main board and the adapters installed in the measurement probe plugs. The modifications consisted mainly of improving the filtering of signals from the device through the cabling and shielding places on the motherboard, which were the

largest source of EMI. In particular, long signal lines and high-frequency lines, where additional capacitors have been added to smooth the edges. The measurement probe adapters are equipped with appropriately selected ferrite beads.

Conclusions

The task aimed to miniaturize the functional modules of the system, thus ensuring energy optimization. The existing diagram of the device's motherboard has been completely remodeled regarding the power supply method. Each circuit in the new design can remotely control the power supply. Critical circuits, i.e., the STM32H7 microcontroller and the ESP32 WiFi communication board, are powered by the high-efficiency LMR12020 converter operating at a frequency of 2MHz throughout the device tests. In contrast, the power supply to the UST and EIT measurement cards can be disconnected during breaks between subsequent measurements, which will significantly reduce consumption—energy stored in batteries. The new design also changed the way of generating high voltage. The latest model of HV converters necessary to develop the ultrasonic signal excitation of the phased measuring head works in SEPIC technology, thanks to which these converters operate with much higher current efficiency and voltage stability than the previously used NMT1272SC compact converters with galvanic isolation. The temperature characteristics depending on the load of the new LT3958 converters are also much better and more stable. Despite the better properties of SEPIC converters, installing a symmetrical isolated converter PDQE15-Q24-D24-D on the motherboard is possible. This converter differs from the previously used one, but it also works more stably than the NMT1272 converters. The new design of the motherboard also has an integrated BMS (Battery Management System) for four 18650 battery cells, necessary for energy optimization of the charging process. Additionally, the motherboard is equipped with a Li-Ion battery charger made using the LTC4006EGN-4 system presented in the previous stage of this project. The final selection of the HV converter will be made during head energy consumption tests.

References

Nowakowski, J., Ostalczyk, P., Sankowski, D. (2017). Application of fractional calculus for modeling of two-phase gas/liquid flow system. Informatyka, Automatyka, Pomiary w Gospodarce i Ochronie Środowiska – IAPGOŚ, 7(1): 42–45.

Romanowski, A., Łuczak, P., Grudzień, K. (2019). X-ray Imaging Analysis of Silo Flow Parameters Based on Trace Particles Using Targeted Crowdsourcing. Sensors, 19(15): 3317.

Rymarczyk, T., Kłosowski, G. (2019). Innovative methods of neural reconstruction for tomographic images in the maintenance of tank industrial reactors. Eksploatacja i Niezawodność – Maintenance and Reliability, 21(2): 261–267.

Rymarczyk, T., Kozłowski, E., Kłosowski, G., Niderla, K. (2019). Logistic Regression for Machine Learning in Process Tomography. Sensors, 19: 3400.

Rymarczyk, T., Szumowski, K., Adamkiewicz, P., Tchórzewski, P., Sikora, J. (2018). Moisture Wall Inspection Using Electrical Tomography Measurements. Przegląd Elektrotechniczny, 94: 97–100.

Soleimani, M., Mitchell, C.N., Banasiak, R., Wajman, R., Adler, A. (2009). Four-dimensional electrical capacitance tomography imaging using experimental data. Progress in Electromagnetics Research, 90: 171–186.